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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/824,978	04/02/2001	Kevin J. McGrath	5500-66000	1318

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Lawrence J. Merkel
Conley, Rose, & Tayon, P.C.
P.O. Box 398
Austin, TX 78767

EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2183	6

DATE MAILED: 06/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/824,978	MCGRATH ET AL.	
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4/2/01* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _ is/are allowed.

6)☒ Claim(s) *1,11 and 21* is/are rejected.

7)☒ Claim(s) *2-10, 12-20, and 22-30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *4/02/01* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2,4,5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to because

in Fig. 5, "Stack 84" should read -Stack 86--; and in the right lower sub-figure, the second pair of "Operand A" ([63:32] and [31:0]) should read -Operand B--; and

in Fig. 12, inside Segment Registers (1054), between "CS" and "DS", --SS-- should be inserted; Similar problems exist in Figs. 13 and 14.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 2, 3, 12, and 13 are objected to because of the following informalities:

in claim 2, line 5, "(ii)" should read --(iii)--; and

in claim 12, line 6, "(ii)" should read --(iii)--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 11, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Kogge (U.S. Patent No. 5,475,856), herein referred to as Kogge'856.

Referring to claim 1, Kogge'856 discloses as claimed a processor comprising: a first register (IR in processor 1, see Fig. 3) configured to store a first target address (note instruction register IR inherently stores a fetched instruction containing a next instruction target address information); a

second register (IR in one of processors 2-N, see Fig. 3) configured to store a second target address (note as set forth above, instruction register IR inherently stores a fetched instruction containing a next instruction target address information); and an execution core (see Fig. 3, the processor comprising processors 1-N, se also col. 4, lines 38-40) coupled to the first register (IR in processor 1, see Fig. 3) and the second register (IR in one of processors 2-N, see Fig. 3), wherein the execution core is configured, responsive to a first instruction (see Col. 6, lines 21-22, and lines 38-40 when the processor 1 functions as a controller), to: (i) select the first target address from the first register (IR in processor 1, see Fig. 3) as a next program counter address if a first operating mode (this is the situation when the SIMD mode is active, see Fig. 1a and see also col. 6, lines 34-37) is active in the processor, and (ii) select the second target address from the second register (IR in one of processors 2-N, see Fig. 3) as the next program counter address if a second operating mode (this is the situation when the MIMD mode is active, see also col. 8, lines 52-56 regarding a processor (one of the processors 2-N, see Figs. 1b and 3), proceeds to fetch instructions as an individual processor) is active in the processor.

Referring to claim 11, Kogge'856 discloses as claimed an apparatus comprising: a first storage location (IR in processor 1, see Fig. 3) corresponding to a first register, the first storage location storing a first target address (note instruction register IR inherently stores a fetched instruction containing a next instruction target address information); a second storage location (IR in one of processors 2-N, see Fig. 3) corresponding to a second register, the second storage location storing a second target address (note as set forth above, instruction register IR inherently stores a fetched instruction containing a next instruction target address information); and a processor (see Fig. 3, the processor comprising processors 1-N, se also col. 4, lines 38-40) coupled to the first storage location and the second storage location, wherein the processor is configured, responsive to a first instruction (see Col. 6, lines 21-22, and lines 38-40 when the processor 1 functions as a controller), to: (i) select the first target address from the first storage location (IR in processor 1, see Fig. 3) as a next program counter address if a first operating mode (this is the situation when the SIMD mode is active, see Fig. 1a and see also col. 6, lines 34-37) is active, and (ii) select the second target address from the second storage location (IR in one of processors 2-N, see Fig. 3) as

the next program counter address if a second operating mode (this is the situation when the MIMD mode is active, see also col. 8, lines 52-56 regarding a processor (one of the processors 2-N, see Figs. 1b and 3), proceeds to fetch instructions as an individual processor) is active.

Referring to claim 21, Kogge'856 discloses as claimed a method comprising: selecting a first target address from a first register (IR in processor 1, see Fig. 3) as a next program counter address responsive to a first operating mode (this is the situation when the SIMD mode is active, see Fig. 1a and see also col. 6, lines 34-37) during execution of a first instruction (see Col. 6, lines 21-22, and lines 38-40 when the processor 1 functions as a controller); and selecting a second target address from a second register (IR in one of processors 2-N, see Fig. 3) as the next program counter address responsive to a second operating mode (this is the situation when the MIMD mode is active, see also col. 8, lines 52-56 regarding a processor (one of the processors 2-N, see Figs. 1b and 3), proceeds to fetch instructions as an individual processor) during execution of the first instruction (since the first instruction in processor 1 determines either SIMD or MIMD mode, see also Col. 6, lines 21-22, and lines 38-40 when the processor 1 functions as a controller and col. 13, lines 25-27) .

Allowable Subject Matter

5. Claims 2, 3, 12, and 13 would be allowable if rewritten to overcome the objection(s), set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

6. Claims 4-10, 14-20, and 22-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure wherein Hasebe et al.'482 also discloses a processor comprising a multiple mode microprogram controller having a first (program execution) mode, second (reset, or stop) mode; and a third (program transfer) mode; Wooten'299 also discloses a multiple mode processor including virtual system mode by allowing to operate

concurrently on different segment registers; and Blomgren et al.'918 discloses a dual-instruction set CPU having shared register for storing data before switching to the alternate instruction set. Using CISC and RISC instruction sets can be considered as having different operation modes in the system as claimed.

Contact Information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (703) 308-7600. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (703) 305-9712. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **TC 2100 receptionist whose telephone number is (703) 305-3900.**

8. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into

the Group at fax number: 703-872-9306.

This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER
May 27, 2004